FIELD EFFECT TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application 60/578,963 filed Jun. 10, 2004.

BACKGROUND OF THE INVENTION

Conventional integrated circuits are fabricated utilizing a number of basic processing steps such as deposition, doping, etching, photolithography and the like. The processes are utilized to form various device structures, such as gates, drains, sources and the like, that makeup a given integrated circuit. Continued advancements in semiconductor fabrication techniques enable continued improvements in device structure of the integrated circuits.

Improvements in the device structure results in improved devices. For example, reducing the channel length of a transistor may result in increased switching speed, reduced power consumption and the like. In the conventional art, processes such as doping, photolithography and the like typically determine the minimum feature size of device structures. For example, a photolithography process typically defines the source and drain regions and therefore the channel length of a transistor.

However, the minimum feature size of structures formed utilizing a photolithography process has reached a limit due to the wavelength of the light used to activate the photoresist. Accordingly, continued scaling of semiconductor devices has become problematic.

SUMMARY OF THE INVENTION

Embodiments of the present invention relate to field effect transistors and methods of manufacturing the devices, wherein a photolithography process does not limit the minimum feature size of the gate and channel length. In one embodiment, a field effect transistor (FET) includes a first semiconductor layer, a first dielectric layer, a second semiconductor layer, a second dielectric layer and a third semiconductor layer. The first dielectric layer may be disposed upon the first semiconductor layer, wherein the first semiconductor layer has a first conductivity type. The second semiconductor layer, having a second conductivity type, may be disposed upon the first dielectric layer. The second dielectric layer may be disposed upon the second semiconductor layer. The third semiconductor layer, having a first conductivity type, may be disposed upon the first semiconductor layer between a first and second portion of the first dielectric layer, a first and second portion of the second semiconductor layer and a first and second portion of the second dielectric layer. The FET may also include a third dielectric layer disposed between the third semiconductor layer and the first and second portions of the second semiconductor layer.

In another embodiment, a method of fabrication a FET includes depositing a first dielectric layer upon a first semiconductor layer. A second semiconductor layer is deposited upon the first dielectric layer. A second dielectric layer is deposited upon the second semiconductor layer. A trench is etched through the second dielectric layer, the second semiconductor layer and the first dielectric layer. A third semiconductor is deposited in the trench. The first and third semiconductor layers may have a first conductivity type. The second semiconductor layer may have a second conductivity type.

Embodiments of the present invention also advantageously provide a FET having a gate (e.g., second semiconductor layer) thickness that is a function of a thin film deposition process. The channel length of the FET is advantageously a function of the gate thickness. Accordingly, a photolithography process does not limit the minimum feature size of the channel of the FET.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention are illustrated by way of example and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

FIG. **1** shows a block diagram of a field effect transistor (FET), in accordance with one embodiment of the present invention.

FIG. **2** shows a block diagram of a FET, in accordance with another embodiment of the present invention.

FIG. **3** shows a graph of space charge thickness versus gate-to-source voltage (V_{GS}) for a FET, in accordance with an exemplary embodiment of the present invention.

FIG. **4** shows a flow diagram of steps in a method of fabricating a field effect transistor (FET), in accordance with one embodiment of the present invention.

FIG. **5** shows a sectional view block diagram of a FET, in accordance with another embodiment of the present invention.

FIG. **6** shows a sectional view block diagram of a FET, in accordance with another embodiment of the present invention.

FIG. **7** shows a sectional view block diagram of a FET, in accordance with another embodiment of the present invention.

FIG. **8** shows a block diagram of a FET, in accordance with another embodiment of the present invention.

FIGS. **9**A and **9**B show a flow diagram of steps in a method of fabricating a FET, in accordance with another embodiment of the present invention.

FIG. **10** shows a graph of depletion region (e.g., space charge) thickness versus gate oxide thickness for FETs, in accordance with exemplary n-channel embodiments of the present invention.

FIG. **11** shows a graph of depletion region (e.g., space charge) thickness versus gate oxide thickness for FETs, in accordance with exemplary p-channel embodiments of the present invention.

FIG. **12** shows a graph of channel resistance versus channel doping for FETs, in accordance with exemplary embodiments of the present invention.

FIG. **13** shows a sectional view block diagram of a complimentary FET, in accordance with one embodiment of the present invention.

FIGS. **14**A, **14**B, **14**C and **14**D show a flow diagram of steps in a method of fabricating a complementary FET, in accordance with one embodiment of the present invention.

FIG. **15** shows a sectional view block diagram of a FET, in accordance with one embodiment of the present invention.

FIGS. **16**A and **16**B show a flow diagram of steps in a method of fabricating a FET, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be